Structural Modeling for multiplexer 4 : 1 using three 2:1 mux

First design 2 : 1 mux

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-- Company:

-- Engineer:

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-- Create Date: 15:23:46 09/24/2015

-- Design Name:

-- Module Name: mux2to1 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating

---- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity mux2to1 is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

s : in STD\_LOGIC;

y : out STD\_LOGIC);

end mux2to1;

architecture Behavioral of mux2to1 is

begin

y<= (not s and a )or( s and b);

end Behavioral;

Now design mux 4 to 1 using three 2:1 mux

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-- Company:

-- Engineer:

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-- Create Date: 15:28:11 09/24/2015

-- Design Name:

-- Module Name: mux4to1 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

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---- Uncomment the following library declaration if instantiating

---- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity mux4to1 is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

c : in STD\_LOGIC;

d : in STD\_LOGIC;

s1 : in STD\_LOGIC;

s0 : in STD\_LOGIC;

y : out STD\_LOGIC);

end mux4to1;

architecture Behavioral of mux4to1 is

component mux2to1 is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

s : in STD\_LOGIC;

y : out STD\_LOGIC);

end component;

signal y1,y2: std\_logic;

begin

mux1 : mux2to1 port map (a,b,s0,y1);

mux2 : mux2to1 port map (c,d,s0,y2);

mux3 : mux2to1 port map (y1,y2,s1,y);

end Behavioral;







